Section A: Basic Information

1. Applicant Details

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Academic Title: Senior Associate Professor

2. Project Details

Titile: High-accuracy and energy-efficient time synchronization immune to floating-point precision loss in wireless sensor networks

Keywords: Synchronization; energy Efficiency; wireless sensor networks; Internet of Things; floating-point arithmetic; Bresenham's algorithm.

Scholarship types willing to accept: Full Scholarship

3. Details of the Supervisors

					No.			
Туре	Name	%	Email	Department/Institution	of	Mentor	Biographical Sketch	1
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Principal	Kyeong Soo Kim	40 Kyeongsoo.Kim@xjtlu.edu.cr	Department of Communications and Networking / XJTLU	4	Kyeong Soo (Joseph) Kim received PhD degree in Electronics Engineering from Seoul National University. He has more than ten years of industrial research and international standardization experiences. He has served many international conferences as committee member and publicity chair and publicity chair and published over 100 papers (4 best/outstanding/excellent paper awards) together with 37 standard contributions with 13 US patents (7 issued and 6 pending). Before joining XJTLU in 2014, he worked with Washington University of Missouri-St. Louis, Lucent Technologies Bell Labs, STMicroelectronics, Stanford Networking Research Center in US and Swansea University in UK. He is a senior member of IEEE and a member of IET.
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UoL Co-	Jeremy S. Smith	30	J.S.Smith@liverpool.ac.uk	Department of Electrical Engineering and Electronics / University of Liverpool	22	Jeremy S. Smith received the B.Eng. degree (Hons.) in Engineering Science and the Ph.D. degree in electrical engineering from the University of Liverpool (UoL) in 1984 and 1990, respectively. From 1984 to 1988, he was conducting research on image processing and robotic systems in the Dept. of EEE, UoL. He has been working as a Lecturer, and a Reader with the Dept. of Electrical Engineering and Electronics since 1988. He has been holding a Professorship in electrical engineering at UoL, since 2006. His research interests include automated welding, robotics, image processing, adaptive control, digital systems, embedded computer systems, computer networks and the IoT. He is a member of both the IEEE and the IET.
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XJTLU Co- supervisor	Ye Liu	30Ye.Liu02@xjtlu.e	du.cn Department of Communications and Networking / XJTLU	0	from City University of Hong Kong. Before joining XJTLU as an assistant professor, he worked as an intern at Nokia Bell Labs (France), a postdoc at Loughborough University, a postdoc at the University of Oxford, and a Lecturer at Coventry University. He has published in high-quality journals such as IEEE Journal of Selected Topics in Signal Processing, IEEE/ACM Transactions in Networking, IEEE Communications Letters, IEEE Wireless Communication Letters, etc. He has secured a research development fund (RDF). His main research interests are signal processing and resource allocation in wireless communication
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Section B: The Proposal

1.Abstract

High-accuracy and energy-efficient time synchronization is important to asymmetric WSNs, where a head node is equipped with high-end processor(s) and supplied power from outlet, but sensor nodes are equipped with low-end processors and battery-powered; their applications include fine-grained localization/tracking and distributed surveillance/sensing in civil and military applications. Through our prior works, we have established a theoretical foundation for high-accuracy and energy-efficient time synchronization for asymmetric WSNs based on the reverse two-way message exchange, but the experimental results based on a real testbed show the negative effect of limited floating-point precision on time synchronization. In this project, we investigate and propose time synchronization algorithms that can avoid the effect of limited floating-point precision and thereby provide high-accuracy time synchronization even at resource-constrained platforms like WSN sensor nodes and IoT devices.

2.Research Background

Noting that in a typical WSN, a head node is equipped with powerful processor(s) and supplied power from outlet, while sensor nodes are equipped with low-end processors and battery-powered, we have been investigating the issue of energy-efficient time synchronization with focus on sensor nodes; we have not

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only proposed energy-efficient WSN time synchronization schemes based on the reverse asymmetric time synchronization framework and evaluated their performance [6]–[10] but also applied them to optimal message bundling and network security [3]–[5].

As shown in Fig. 1, there are two approaches to the time synchronization based on the reverse asymmetric time synchronization framework, i.e., one based on reverse one-way message dissemination (BATS [8]) and the other based on reverse two-way message exchange (EE-ASCFR [10]). In BATS, all synchronization tasks but timestamping are moved from resource-constrained sensor nodes to the head but, due to the lack of two-way message exchange, the propagation delay cannot be compensated for. EE-ASCFR, on the other hand, can compensate for the propagation delay and enable the receiving-only operation for a long period of time as shown in Fig. 2, where the base station broadcasts beacons to the sensor nodes in the enemy territory, which are just receiving them for frequency synchronization and control information to prevent from being detected by the enemy; the data measured by the sensor nodes are finally collected by drones hovering the area.

The key idea of EE-ASCFR is the separation of time synchronization into the clock frequency synchronization at sensor nodes and the clock offset estimation at the head. Our investigation on a real testbed, however, reveals that its performance on sensor nodes is not up to that predicted from simulations due to the floating-point division and the recursive nature of the clock estimation incurring substantial precision loss with 32-bit single precision as shown in Fig. 3 [9].

We have proposed AHTS [9] and BATS to address the issue of the limited precision floating-point arithmetic based on the idea of relieving resource-constrained sensor nodes of all time synchronization tasks but timestamping. Moving all time synchronization tasks but timestamping to the head, however, would increase the number of message transmissions from sensor nodes and thereby make both AHTS and BATS not only unscalable in case of multi-hop scenarios but also unsuitable for the scenario shown in Fig. 2.

3. Objectives and Research Questions

The aim is to study high-accuracy and low-complexity energy-efficient time synchronization for sensor nodes based on platforms with lower power and computational resources, whose target applications include fine-grained localization/tracking and distributed surveillance/sensing in both civil and military applications.

The major objectives are:

• To propose high-accuracy and energy-efficient time synchronization algorithms, which are immune to floating-point operation errors on resource-constrained WSN/IoT platforms.

• To evaluate their performance through mathematical analyses and experiments on a real testbed..

The fundamental research question is how to achieve accurate WSN time synchronization in an energyefficient way under the constraint of low computational complexity of sensor nodes; the answer to this question is critical because it is directly related to the uninterrupted operation time and maintenance cost of sensor nodes as well as the accuracy of measurement timing.

4. Research Methods and Approach

In [2] and [1], to avoid the effect of limited floating-point precision, we propose a clock skew compensation algorithm based on the Bresenham's line drawing algorithm [12]---i.e., an incremental error algorithm implementable using only integer addition, subtraction, and bit shifting---on the basis that the clocks in digital communication systems are basically discrete counters.

If D/A is the inverse of a clock frequency ratio estimated based on two positive integers D and A, which represent interdeparture and interarrival times of packets or their cumulative sums from the previous synchronizations as suggested in [11], we can obtain the skew-compensated increment of the hardware clock as shown in Fig. 4 (a) using the Bresenham's algorithm, where Δa and Δb are set to A and D, respectively: At each tick of the sensor node's clock, we can estimate the reference clock value using the horizontal (M_1) and diagonal (M_2) movements, which are selected based on the value of an error term updated recursively through simple integer arithmetic. Unlike the line drawing, however, the skew

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compensation does not need all the intermediate points between the origin and the point under consideration (i.e., i in Fig. 4 (a)), so we cannot use the Bresenham's algorithm as it is, especially when D and A are large numbers and there are sparse events/measurements.

In [2], we extend the Bresenham's algorithm based on a backward-reachable set and a modified error term over the set as shown in Fig. 4 (b): Instead of starting from the origin, we jump to i and estimate the bounds on the value of a skew-compensated clock (iD/A) calculated based on the limited floating-point precision at sensor nodes, which determine the backward-reachable set covering the whole range of possible values of i D/A; then, we apply the extended Bresenham's algorithm from the leftmost point of the set until the x coordinate of the point from the algorithm becomes i.

Fig. 4 (b) shows that the number of steps of the algorithm depends on the bounds on the value of skewcompensated clock, which are affected by the floating-point operation errors due to precision loss. In [1], we revisit the main Theorem of [2] and provide practical as well as theoretical bounds on the initial value of skew-compensated clock based on a systematic analysis of the errors of floating-point operations with the floating-point formats defined in the IEEE standard [18].

In the proposed research, we will improve the clock skew compensation algorithm in the following aspects:

First, we will refine the quantitative analysis of the floating-point operation errors and their impact on the clock skew compensation to derive tighter practical bounds on the initial value of skew-compensated clock, which reduces the number of steps required by the extended Bresenham's algorithm.

Second, we will propose a new algorithm based on the extended Bresenham's algorithm with vertical movements and a new error term, which does not require the backward-reachable set and the bounds on the initial value of skew-compensated clock as an initial condition of the algorithm. Fig. 5 shows a sketch of this algorithm.

Third, for the experimental verification of the proposed algorithms, we will upgrade the testbed shown in Fig. 6, which is based on TelosB motes [19] running TinyOS [20]; specifically, we plan to develop WSN/IoT nodes based on development boards with ESP32 or STM32 SOC microcontrollers with LoRa and GPS modules, which would enable the operations in a much longer distance than typical Zigbee-based ones. In this case, we would be no longer limited to specific software and hardware and also have much more economical experimental platforms for the performance verification.

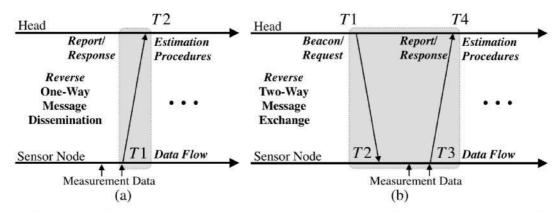


Fig. 1. Reverse asymmetric time synchronization based on (a) one-way message dissemination and (b) two-way message exchange, both with optional bundling of measurement data [8].

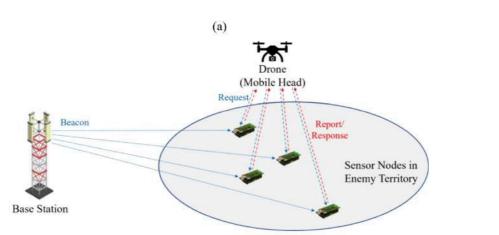


Fig. 2. Example scenario for joint intelligence, surveillance, and reconnaissance with drones in battle fields based on EE-ASCFR [10].

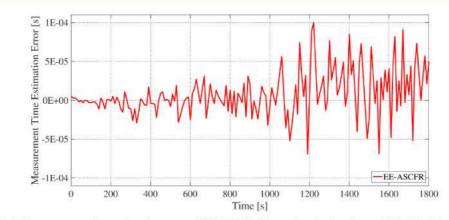


Fig. 3. Measurement time estimation errors of EE-ASCFR with synchronization interval (SI) of 1 s [9].



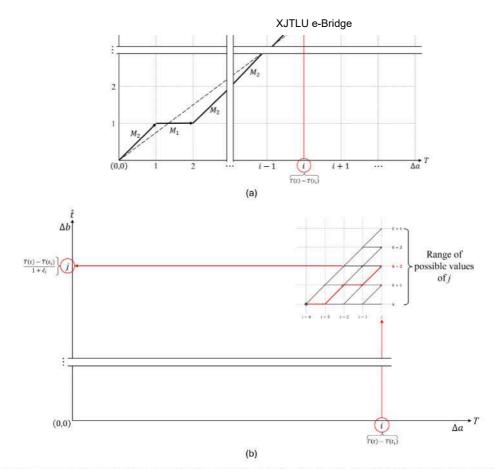


Fig. 4. Clock skew compensation based on the Bresenham's algorithm for $\Delta a/\Delta b < 1$ [2]: (a) The original and (b) the extended algorithm.

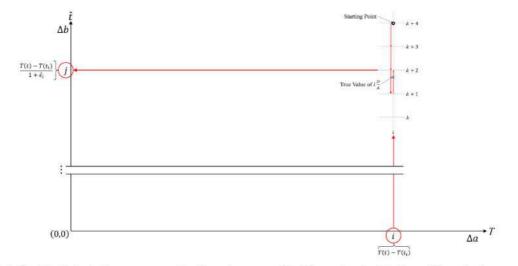


Fig. 5. Sketch of clock skew compensation based on a modified Bresenham's algorithm with vertical https://ebridge.xjtlu.edu.cn/urd/sits.urd/run/SIW_YGSL.start_url?BB5DA0D7FA1D48B2GwSwHCGC2kGkqbuK-tcdsbvjL8MzdScV12L2SwRR5Q... 8/13

movements for $\Delta a / \Delta b < 1$.

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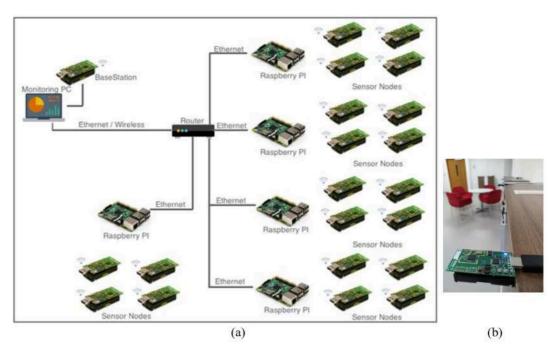


Fig. 6. IoT/WSN testbed under operation: (a) An overview and (b) actual deployment in the Lab.

5.List of Abbreviations

- AHTS: Asymmetric High-precision Time Synchronization.
- BATS: Beaconless Asymmetric energy-efficient Time Synchronization.
- EE-ASCFR: Energy-Efficient time synchronization scheme based on Asynchronous Source Clock Frequency Recovery and reverse two-way message exchange.
- FTSP: Flooding Time Synchronization Protocol.
- IoT: Internet of Things.
- SCFR: Source Clock Frequency Recovery.
- WSN: Wireless Sensor Network.

6. List of Previous Publications

1. S. Kang and K. S. Kim, "Theoretical and practical bounds on the initial value of clock skew compensation algorithm immune to floating-point precision loss for resource-constrained wireless sensor nodes," Fiber and Integrated Optics, vol. 43, no. 3, pp. 111–121, Jun. 24, 2024.

2. K. S. Kim and S. Kang, "Clock skew compensation algorithm immune to floating-point precision loss," IEEE Commun. Lett., vol. 26, no. 4, pp. 902–906, Apr. 2022.

3. S. Li, K. S. Kim, L. Zhang, X. Huan, and J. Smith, "Energy-efficient message bundling with delay and synchronization constraints in wireless sensor networks," Sensors, vol. 22, no.14:5276, Jul. 2022.

4. X. Huan, K. S. Kim, and J. Zhang, "NISA: Node identification and spoofing attack detection based on clock features and radio information for wireless sensor networks," IEEE Trans. Commun., vol. 69, no. 7, pp. 4691–4703, Jul. 2021.

5. X. Huan, K. S. Kim, S. Lee, and M. K. Kim, "Optimal message bundling with delay and synchronization constraints in wireless sensor networks," Sensors, vol. 19, no. 18:4027, Sep. 2019.

6. X. Huan, K. S. Kim, S. Lee, E. G. Lim, and A. Marshall, "Improving multi-hop time synchronization performance in wireless sensor networks based on packet-relaying gateways with per-hop delay compensation," IEEE Trans. Commun., vol. 69, no. 9, pp. 6093–6105, Sep. 2021.

7. X. Huan and K. S. Kim, "Per-hop delay compensation in time synchronization for multi-hop wireless sensor networks based on packet-relaying gateways," IEEE Commun. Lett., vol. 24, no. 10, pp. 2300–2304, Oct. 2020.

8. X. Huan, K. S. Kim, S. Lee, E. G. Lim, and A. Marshall, "A beaconless asymmetric energy-efficient time synchronization scheme for resource-constrained multi-hop wireless sensor networks," IEEE Trans. Commun., vol. 68, no. 3, pp. 1716–1730, Mar. 2020.

9. X. Huan and K. S. Kim, "On the practical implementation of propagation delay and clock skew compensated high-precision time synchronization schemes with resource-constrained sensor nodes in multi-hop wireless sensor networks," Computer Networks, vol. 166, pp. 1–8, Jan. 2020.

10. K. S. Kim, S. Lee, and E. G. Lim, "Energy-efficient time synchronization based on asynchronous source clock frequency recovery and reverse two-way message exchanges in wireless sensor networks," IEEE Trans. Commun., vol. 65, no. 1, pp. 347–359, Jan. 2017.

11. K. S. Kim, "Asynchronous source clock frequency recovery through aperiodic packet streams," IEEE Commun. Lett., vol. 17, no. 7, pp. 1455–1458, 2013.

7.References

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13. IEEE Computer Society, IEEE Std 754[™]-2008, IEEE standard for floating-point arithmetic, Std., Aug. 2008.

14. TelosB datasheet. [Online]. Available: https://www.willow.co.uk/TelosB_Datasheet.pdf

15. TinyOS. [Online]. Available: https://github.com/tinyos/tinyos-main

16. Contiki-NG: The OS for next generation IoT devices. [Online]. Available: https://github.com/contiki-ng/contiki-ng

17. M. Maróti, B. Kusy, G. Simon, and Á. Lédeczi, "The flooding time synchronization protocol," Proc. SenSys'04, pp. 39–49, Baltimore, MD, USA, Nov. 2004.

8. Timeline of the Proposed Research

Tasks	Year 1				Year 2				Year 3				
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	
1. Time synchronization schemes immune to floating-point precision loss													
Investigation of time synchronization													
Network emulation/simulation													
2. IoT/WSN testbed													
Upgrade of the IoT/WSN testbed													
Performance evaluation													
3. Dissemination of Results													
Exchange of ideas/early results/feedback													
Final report													

Milestones for each task

- 1. Time synchronization schemes immune to floating-point precision loss.
 - Theoretical investigation of energy-efficient and low-complexity time synchronization
 immune to floating-point precision loss.
 - Study of the proposed schemes based on network emulation/simulation.
- 2. IoT/WSN testbed.
 - · Upgrade of the IoT/WSN testbed shown in Fig. 6.
 - Evaluation of the proposed time synchronization schemes.
- 3. Dissemination of Results.
 - Exchange of ideas, early results, and feedback through conferences/workshops/seminars.
 - A final report summarizing outcomes from the project and areas for further investigation.

9. Potential Contribution and Impact of the Proposed Research

The clock skew compensation runs continuously during the lifetime of a sensor node and, unlike other operations like sensing and localization, its impact on time synchronization could be cumulative as shown in Fig. 3, which clearly indicates the importance of clock skew compensation algorithms immune to floating-point precision loss, especially for sensor nodes based on platforms with lower computational resources.

The outcomes from the proposed research will be quite unique and innovative in that, to the best of our knowledge, there have been no other works systematically investigating and addressing the issue of floating-point precision loss in time synchronization on resource-constrained WSN platforms with 32-bit single precision based on a quantitative analysis, except our preliminary works of [1] and [2] discussed in detail in Section 4.

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Given the ever-increasing number of WSN and IoT devices and applications based on them, the proposed study on energy-efficient and low-complexity time synchronization has a practical importance in the broader aspects as follows:

• The time synchronization schemes from this study running on a myriad of battery-powered WSN and IoT devices could enlarge their operation times.

• The low complexity requirement of the proposed time synchronization schemes could simplify the implementation of WSN and IoT devices and thereby reduce their costs.

• The accurate time synchronization provided by the proposed time synchronization schemes could improve the quality of the information inferred from sensed data as well as the network operation.

• The receiving-only operation of sensor nodes for a long period of time enabled by the proposed time synchronization schemes makes it feasible to deploy WSN nodes in enemy territories for military scenarios as shown in Fig. 2.

10.Risk Mitigation Strategy

The proposed research program is based on the years of our investigation on energy-efficient WSN time synchronization schemes and their applications (i.e., [1]–[11]); especially, the seed works in [2] and [1] provide a solid theoretical foundation for the current proposal as discussed in Section 4.

As for the experiments on a real IoT/WSN testbed, we already have the 21-node WSN testbed under operation in our Lab at XJTLU again as discussed in Section 4; the experience of implementing and running various time synchronization schemes—i.e., EE-ASCFR, AHTS, BATS, and FTSP [17]—on the WSN testbed would be of great help to the experimental verification of the time synchronization algorithms resulting from the proposed research.

Also, the said work on energy-efficient WSN time synchronization schemes and their applications has been done in close collaboration with both domestic and foreign colleagues, including Dr. Xintao Huan at Beijing Institute of Technology (BIT), Prof. Sanghyuk Lee at New Uzbekistan University, Uzbekistan, Prof. Alan Marshall at the University of Liverpool, UK, Prof. Eng Gee Lim at XJTLU, and Prof. Hahng-Yun Chu at Chungnam National University, Korea, which the current proposal will continue to exploit through consulting visits and seminars.

11.Provision of Training

Given the advanced and challenging nature of the research we propose, we need a PhD student who has good research experience and programming skills. In this regard, ongoing FMPs and FYPs are truly good opportunities for us to test and identify potential candidates for this research proposal, which was the case for most of the past and ongoing RDF/PGRS projects.

In case the PhD student still needs to improve his/her programming skills, we will use on-line courses provided by coursera (https://www.coursera.org/) as we did with other PhD, master's, and SURF students. Note that the on-line courses provided by coursera require enrollment and completion of all the assignments to get a certificate.

As for general research methodologies for carrying out a PhD project, the student will be trained through weekly supervisory meetings as well as the workshops and seminars provided by XJTLU GSO.

12.Expected Outputs

	Number		Number
Journal Paper	2	Invention	1
Conference Paper	3	Utility Model	0
Book	0	Design Patent	0
		Software Copyright	0

Other Research Impact Measures

N/A

13.Research Support Received

Internal/External	Funding Scheme	Project Title	Year of Award	Ы	Remaining Amount	
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Does your PGRS project require additional research costs, such as field trip expenses, highperformance workstations, consumable costs, or extra conference funds exceeding university standards?

No

N/A

What external funding will you seek?

National Natural Science Fund of China Research Fund for International Scientists.

14. Ethical Requirements of Research Projects Involving Humans and/or Animals

No

15. Additional information (if any)

N/A

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